

Appl. No. 10/709,854
Amtd. dated November 29, 2004
Reply to Office action of September 09, 2004

Amendments to the Claims:

- 1 (Currently amended) An electrically programmable non-volatile memory-cell array, comprising:
 - 5 a semiconductor substrate of first conductivity type;
 - a pair columns of spaced apart source/drain (S/D) regions defined on said semiconductor substrate;
 - a channel region between two of said source/drain (S/D) regions;
 - 10 a first dielectric layer disposed on said source/drain (S/D) regions;
 - an columns of assistant-gate gates stacked on said first dielectric layer, wherein each of said assistant-gate gates has a top surface and sidewalls, wherein at least one end of each said columns of assistant gates partially overlaps with a doped pickup well formed in said semiconductor substrate, and wherein a bit line voltage is provided to said doped pickup well;
 - 15 a second dielectric layer comprising a charge-trapping layer uniformly disposed on said top surface and sidewalls of said assistant gate and disposed on said channel region, wherein said second dielectric layer produces a recessed trough between said source/drain (S/D) regions; and
 - 20 a conductive gate material filling said recessed trough for controlling said channel region rows of word lines laid on said second dielectric layer, said rows of word lines intersecting said columns of assistant gates,
wherein, in operation when programming a memory cell defined by a specific row of said word lines of said electrically programmable non-volatile memory array, only two columns of said assistant-gate gates next to said memory cell is are biased to a voltage V_i that is sufficient to correspondingly induce a corresponding two columns of inversion region regions of second conductivity type in said semiconductor substrate; and wherein said inversion region regions of second conductivity type functions function as a source/drain of said electrically programmable non-volatile memory cell.

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2 (Currently amended) The electrically programmable non-volatile memory-cell array according to claim 1 wherein said first dielectric layer is made of silicon dioxide.

5 3 (Currently amended) The electrically programmable non-volatile memory-cell array according to claim 2 wherein said silicon dioxide is thermally grown.

4 (Currently amended) The electrically programmable non-volatile memory-cell array according to claim 1 wherein said second dielectric layer is a tri-layer dielectric.

10 5 (Currently amended) The electrically programmable non-volatile memory-cell array according to claim 1 wherein said second dielectric layer is an ONO tri-layer, and said charge-trapping layer is a silicon nitride layer sandwiched between a bottom oxide layer and a top oxide layer.

15 6 (Currently amended) The electrically programmable non-volatile memory-cell array according to claim 1 wherein said second dielectric layer is a bilayer dielectric.

20 7 (Currently amended) The electrically programmable non-volatile memory-cell array according to claim 1 wherein said assistant gate is made of polysilicon.

8 (Currently amended) The electrically programmable non-volatile memory-cell array according to claim 1 wherein said ~~conductive gate material~~ word line comprises polysilicon.

25 9 (Currently amended) The electrically programmable non-volatile memory-cell array according to claim 1 wherein said ~~conductive gate material~~ word line is metal word line.

10-17 (Canceled)